Claims

What is claimed is:

1. A system for generating an output clock signal having a controllable duty cycle from an input clock signal, comprising:

a duty cycle corrector circuit structured to generate the output clock signal from the input clock signal, the duty cycle corrector circuit being structured to transition the output clock signal to a first logic level responsive to a first transition of the input clock signal after a first delay that corresponds to a first control signal, the duty cycle corrector circuit being structured to further transition the output clock signal to a second logic level that is different from the first logic level responsive to a second transition of the input clock signal that is different from the first transition of the input clock signal after a second delay that corresponds to a second control signal;

a duty cycle indicating circuit coupled to receive the output clock signal from the duty cycle corrector circuit and to generate a duty cycle feedback signal corresponding thereto; and

a control circuit coupled to the duty cycle indicating circuit and the duty cycle corrector circuit, the control circuit being structured to generate the first and second control signals as a function of the duty cycle feedback signal so that the first and second delays are selected to cause the output clock signal to have a predetermined duty cycle.

2. The system of claim 1 wherein the duty cycle indicating circuit comprises an integrator circuit coupled to receive the output clock signal from the duty cycle corrector circuit and to generate as the duty cycle feedback signal a signal corresponding to the integral of the output clock signal with respect to time.

3. The system of claim 2 wherein the integrator circuit comprises:

an inverter having an output terminal and an input terminal coupled to receive the output clock signal; and

a capacitor coupled to the output terminal of the inverter.

4. The system of claim 3 wherein the inverter comprises:

a first transistor coupled to the capacitor;

a second transistor coupled to the capacitor;

a current source coupled in series with the first transistor; and

a current sink coupled in series with the second transistor.

5. The system of claim 1 wherein the duty cycle corrector circuit comprises:

a first switch having a control input coupled to receive the input clock signal, the first switch being closed responsive to a first logic level of the input clock signal;

a second switch having a control input coupled to receive the input clock signal, the second switch being closed responsive to a second logic level of the input clock signal;

a first current regulating device coupled in series with the first switch between a first supply voltage and an output node, the first current regulating device having a control input coupled to receive the first control signal;

a second current regulating device coupled in series with the second switch between the output node and a second supply voltage; the second current regulating device having a control input coupled to receive the second control signal;

a capacitor coupled to the output node; and

a level detector coupled to the output node, the level detector setting the output clock signal to a first logic level responsive to the voltage on the capacitor being greater than a first transition voltage and setting the output clock signal to a second logic level responsive to the voltage on the capacitor being less than a second transition voltage.

6. The system of claim 5 further comprising:

a third switch coupled in parallel with the first current regulating device, the third switch being structured to close responsive to the voltage on the capacitor being charged to at least the first transition voltage; and

a fourth switch coupled in parallel with the second current regulating device, the fourth switch being structured to close responsive to the voltage on the capacitor being discharged to at least the second transition voltage.

7. The system of claim 5 wherein the first and second current regulating devices comprise respective first and second transistors having their gates coupled to receive the first and second control signals, respectively.

8. The system of claim 1 wherein the control circuit comprises:

a transconductance amplifier having a first input coupled to the duty cycle indicating circuit to receive the duty cycle feedback signal therefrom and a second input coupled to a reference voltage, the transconductance amplifier being structured to generate first and second currents through respective first and second output terminals, the first current corresponding to the difference in magnitude between the duty cycle feedback signal and the reference voltage, and the second current corresponding to the difference between a constant current and the first current; and

an adjusting circuit generating the first control signal as a voltage corresponding to the first current and generating the second control signal as a voltage corresponding to the second current.

9. The system of claim 1 wherein the adjusting circuit comprises:

a first transistor having a gate coupled to transconductance amplifier to receive the first current therefrom, a source coupled to a first power supply voltage, and a drain coupled to the gate, the first transistor generating the first control signal at the drain of the first transistor;

a current mirror coupled to the transconductance amplifier to receive the second current therefrom, the current mirror generating a third current that is substantially equal to the second current; and

a second transistor having a gate coupled to current mirror to receive the third current therefrom, a source coupled to a first power supply voltage, and a drain coupled to the gate, the second transistor generating the second control signal at the drain of the second transistor.

10. A duty cycle corrector circuit, comprising:

a first switch having a control input coupled to receive an input clock signal, the first switch being closed responsive to a first logic level of the input clock signal;

a second switch having a control input coupled to receive the input clock signal, the second switch being closed responsive to a second logic level of the input clock signal;

a first current regulating device coupled in series with the first switch between a first supply voltage and an output node, the first current regulating device having a control input coupled to receive a first control signal;

a second current regulating device coupled in series with the second switch between the output node and a second supply voltage; the second current regulating device having a control input coupled to receive a second control signal;

a capacitor coupled to the output node; and

a level detector coupled to the output node, the level detector setting an output clock signal to a first logic level responsive to the voltage on the capacitor being greater than a first transition voltage and setting the output clock signal to a second logic level responsive to the voltage on the capacitor being less than a second transition voltage.

11. The duty cycle corrector circuit of claim 10 wherein the first and second current regulating devices comprise respective first and second transistors having their gates coupled to receive the first and second control signals, respectively.

12. The duty cycle corrector circuit of claim 10 further comprising:

a third switch coupled in parallel with the first current regulating device, the third switch being structured to close responsive to the voltage on the capacitor being charged to at least the first transition voltage; and

a fourth switch coupled in parallel with the second current regulating device, the fourth switch being structured to close responsive to the voltage on the capacitor being discharged to at least the second transition voltage.

13. A memory device, comprising:

an array of memory cells;

an address decoder adapted to receive an address and to specify a location in the array of memory cells corresponding thereto;

a read/write circuit coupling data to and from the specified location in the array of memory cells;

a control logic circuit receiving command signals and generating control signals corresponding thereto; and

a clock generator circuit receiving an input clock signal and generating from the input clock signal an output clock signal having a controllable duty cycle , the clock generator circuit comprising:

a duty cycle corrector circuit structured to generate the output clock signal from the input clock signal, the duty cycle corrector circuit being structured to transition the output clock signal to a first logic level responsive to a first transition of the input clock signal after a first delay that corresponds to a first control signal, the duty cycle corrector circuit being structured to further transition the output clock signal to a second logic level that is different from the first logic level responsive to a second transition of the input clock signal that is different from the first transition of the input clock signal after a second delay that corresponds to a second control signal;

a duty cycle indicating circuit coupled to receive the output clock signal from the duty cycle corrector circuit and to generate a duty cycle feedback signal corresponding thereto; and

a control circuit coupled to the duty cycle indicating circuit and the duty cycle corrector circuit, the control circuit being structured to generate the first and second control signals as a function of the duty cycle feedback signal so that the first and second delays are selected to cause the output clock signal to have a predetermined delay.

14. The memory device of claim 13 wherein the duty cycle indicating circuit comprises an integrator circuit coupled to receive the output clock signal from the duty cycle corrector circuit and to generate as the duty cycle feedback signal a signal corresponding to the integral of the output clock signal with respect to time.

15. The memory device of claim 14 wherein the integrator circuit comprises:

an inverter having an output terminal and an input terminal coupled to receive the output clock signal; and

a capacitor coupled to the output terminal of the inverter.

16. The memory device of claim 15 wherein the inverter comprises:

a first transistor coupled to the capacitor;

a second transistor coupled to the capacitor;

a current source coupled in series with the first transistor; and

a current sink coupled in series with the second transistor.

17. The memory device of claim 13 wherein the duty cycle corrector circuit comprises:

a first switch having a control input coupled to receive the input clock signal, the first switch being closed responsive to a first logic level of the input clock signal;

a second switch having a control input coupled to receive the input clock signal, the second switch being closed responsive to a second logic level of the input clock signal;

a first current regulating device coupled in series with the first switch between a first supply voltage and an output node, the first current regulating device having a control input coupled to receive the first control signal;

a second current regulating device coupled in series with the second switch between the output node and a second supply voltage; the second current regulating device having a control input coupled to receive the second control signal;

a capacitor coupled to the output node; and

a level detector coupled to the output node, the level detector setting the output clock signal to a first logic level responsive to the voltage on the capacitor being greater than a first transition voltage and setting the output clock signal to a second logic level responsive to the voltage on the capacitor being less than a second transition voltage.

18. The system of claim 17 further comprising:

a third switch coupled in parallel with the first current regulating device, the third switch being structured to close responsive to the voltage on the capacitor being charged to at least the first transition voltage; and

a fourth switch coupled in parallel with the second current regulating device, the fourth switch being structured to close responsive to the voltage on the capacitor being discharged to at least the second transition voltage.

19. The memory device of claim 17 wherein the first and second current regulating devices comprise respective first and second transistors having their gates coupled to receive the first and second control signals, respectively.

20. The memory device of claim 13 wherein the control circuit comprises:

a transconductance amplifier having a first input coupled to the duty cycle indicating circuit to receive the duty cycle feedback signal therefrom and a second input coupled to a reference voltage, the transconductance amplifier being structured to generate first and second currents through respective first and second output terminals, the first current corresponding to the difference in magnitude between the duty cycle feedback signal and the reference voltage, and the second current corresponding to the difference between a constant current and the first current; and

an adjusting circuit generating the first control signal as a voltage corresponding to the first current and generating the second control signal as a voltage corresponding to the second current.

21. The memory device of claim 13 wherein the adjusting circuit comprises:

a first transistor having a gate coupled to transconductance amplifier to receive the first current therefrom, a source coupled to a first power supply voltage, and a drain coupled to the gate, the first transistor generating the first control signal at the drain of the first transistor;

a current mirror coupled to the transconductance amplifier to receive the second current therefrom, the current mirror generating a third current that is substantially equal to the second current; and

a second transistor having a gate coupled to current mirror to receive the third current therefrom, a source coupled to a first power supply voltage, and a drain coupled to the gate, the second transistor generating the second control signal at the drain of the second transistor.

22. The memory device of claim 13 wherein the memory device comprises a dynamic random access memory.

23. The memory device of claim 22 wherein the memory device comprises a synchronous dynamic random access memory.

24. The memory device of claim 13 wherein the input clock signal comprises a clock signal applied to the memory device from an external source.

25. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a memory device coupled to the processor through the processor bus, the memory device comprising:

an array of memory cells;

an address decoder adapted to receive an address and to specify a location in the array of memory cells corresponding thereto;

a read/write circuit coupling data to and from the specified location in the array of memory cells;

a control logic circuit receiving command signals and generating control signals corresponding thereto; and

a clock generator circuit receiving an input clock signal and generating from the input clock signal an output clock signal having a controllable duty cycle, the clock generator circuit comprising:

a duty cycle corrector circuit structured to generate the output clock signal from the input clock signal, the duty cycle corrector circuit being structured to transition the output clock signal to a first logic level responsive to a first transition of the input clock signal after a first delay that corresponds to a first control signal, the duty cycle corrector circuit being structured to further transition the output clock signal to a second logic level that is different from the first logic level responsive to a second transition of the input clock signal that is different from the first transition of the input clock signal after a second delay that corresponds to a second control signal;

a duty cycle indicating circuit coupled to receive the output clock signal from the duty cycle corrector circuit and to generate a duty cycle feedback signal corresponding thereto; and

a control circuit coupled to the duty cycle indicating circuit and the duty cycle corrector circuit, the control circuit being structured to generate the first and second control signals as a function of the duty cycle feedback signal so that the first and second delays are selected to cause the output clock signal to have a predetermined delay.

26. The computer system of claim 25 wherein the duty cycle indicating circuit comprises an integrator circuit coupled to receive the output clock signal from the duty cycle corrector circuit and to generate as the duty cycle feedback signal a signal corresponding to the integral of the output clock signal with respect to time.

27. The computer system of claim 26 wherein the integrator circuit comprises:

an inverter having an output terminal and an input terminal coupled to receive the output clock signal; and

a capacitor coupled to the output terminal of the inverter.

28. The computer system of claim 27 wherein the inverter comprises:

a first transistor coupled to the capacitor;

a second transistor coupled to the capacitor;

a current source coupled in series with the first transistor; and

a current sink coupled in series with the second transistor.

29. The computer system of claim 25 wherein the duty cycle corrector circuit comprises:

a first switch having a control input coupled to receive the input clock signal, the first switch being closed responsive to a first logic level of the input clock signal;

a second switch having a control input coupled to receive the input clock signal, the second switch being closed responsive to a second logic level of the input clock signal;

a first current regulating device coupled in series with the first switch between a first supply voltage and an output node, the first current regulating device having a control input coupled to receive the first control signal;

a second current regulating device coupled in series with the second switch between the output node and a second supply voltage; the second current regulating device having a control input coupled to receive the second control signal;

a capacitor coupled to the output node; and

a level detector coupled to the output node, the level detector setting the output clock signal to a first logic level responsive to the voltage on the capacitor being greater than a first transition voltage and setting the output clock signal to a second logic level responsive to the voltage on the capacitor being less than a second transition voltage.

30. The computer system of claim 29 further comprising:

a third switch coupled in parallel with the first current regulating device, the third switch being structured to close responsive to the voltage on the capacitor being charged to at least the first transition voltage; and

a fourth switch coupled in parallel with the second current regulating device, the fourth switch being structured to close responsive to the voltage on the capacitor being discharged to at least the second transition voltage.

31. The computer system of claim 29 wherein the first and second current regulating devices comprise respective first and second transistors having their gates coupled to receive the first and second control signals, respectively.

32. The computer system of claim 25 wherein the control circuit comprises:

a transconductance amplifier having a first input coupled to the duty cycle indicating circuit to receive the duty cycle feedback signal therefrom and a second input coupled to a reference voltage, the transconductance amplifier being structured to generate first and second currents through respective first and second output terminals, the first current corresponding to the difference in magnitude between the duty cycle feedback signal and the reference voltage, and the second current corresponding to the difference between a constant current and the first current; and

an adjusting circuit generating the first control signal as a voltage corresponding to the first current and generating the second control signal as a voltage corresponding to the second current.

33. The computer system of claim 32 wherein the adjusting circuit comprises:

a first transistor having a gate coupled to transconductance amplifier to receive the first current therefrom, a source coupled to a first power supply voltage, and a drain coupled to the gate, the first transistor generating the first control signal at the drain of the first transistor;

a current mirror coupled to the transconductance amplifier to receive the second current therefrom, the current mirror generating a third current that is substantially equal to the second current; and

a second transistor having a gate coupled to current mirror to receive the third current therefrom, a source coupled to a first power supply voltage, and a drain coupled to the gate, the second transistor generating the second control signal at the drain of the second transistor.

34. The computer system of claim 25 wherein the memory device comprises a dynamic random access memory.

35. The computer system of claim 34 wherein the memory device comprises a synchronous dynamic random access memory.

36. The computer system of claim 25 wherein the input clock signal comprises a clock signal applied to the memory device from an external source.

37. A method of generating an output clock signal having a controllable duty cycle from an input clock signal, comprising:

charging a capacitor with a charge current responsive to a first edge of the input clock signal;

discharging a capacitor with a discharge current responsive to a second edge of the input clock signal, the second edge having an opposite polarity from the first edge;

detecting when the capacitor has been charged to a first voltage, and, in response thereto, rapidly charging the capacitor to a second voltage;

detecting when the capacitor has been discharged to a third voltage, and, in response thereto, rapidly discharging the capacitor to a fourth voltage;

transitioning the output clock signal to a first logic level responsive to detecting that the capacitor had been charged to the first voltage;

transitioning the output clock signal to a second logic level that is different from the first logic level responsive to detecting that the capacitor had been discharged to the second voltage;

providing a feedback signal indicative of the duty cycle of the output clock signal; and

adjusting the charge current and the discharge current responsive to the feedback signal to control the duty cycle of the output clock signal.

38. The method of claim 37 wherein the act of providing a feedback signal comprises integrating the output clock signal to provide a signal corresponding to the duty cycle of the output clock signal.

39. The method of claim 38 wherein the act of integrating the output clock signal to provide the feedback signal comprises:

charging a second capacitor with a fixed charging current when the output clock signal has one of the first and second logic levels;

discharging the second capacitor with a fixed discharging current when the output clock signal as the other of the first and second logic levels; and

using the voltage on the second capacitor as the feedback signal.

40. The method of claim 37 wherein the acts of charging the capacitor with a charge current and discharging the capacitor with a discharge current comprise coupling the capacitor to respective first and second supply voltages through respective first and second coupling elements each having an impedance determined by a respective first and second control signals, and wherein the act of adjusting the charge current and discharge current responsive to the feedback signal comprises:

generating a first feedback voltage as a function of the feedback signal;

generating the first control signal as a function of the difference between the magnitude of the first feedback voltage and the first power supply voltage;

generating a second feedback voltage as a function of the feedback signal; and

generating the second control signal as a function of the difference between the magnitude of the second feedback voltage and the second power supply voltage.

41. The method of claim 37 wherein the acts of charging the capacitor with a charge current and discharging the capacitor with a discharge current comprise coupling the feedback signal to a transconductance amplifier having first and second output terminals through which respective first and second currents flow, the first current corresponding to the difference in magnitude between the feedback signal and a reference voltage, and second respective current corresponding to the difference between a constant current and the first current; and

adjusting the magnitude of the charge current so that it corresponds to the first current; and

adjusting the magnitude of the discharge current so that it corresponds to the second current.

42. The method of claim 41 wherein the act of adjusting one of the charge current or the discharge current comprises:

generating a third current that is substantially equal to the one of the charge current or the discharge current;

coupling the third current through a circuit element having a control voltage that is proportional to the third current; and

adjusting the one of the charge current or the discharge current responsive to the control voltage.

43. The method of claim 41 further comprising adjusting the magnitude of the reference voltage, thereby adjusting the duty cycle.